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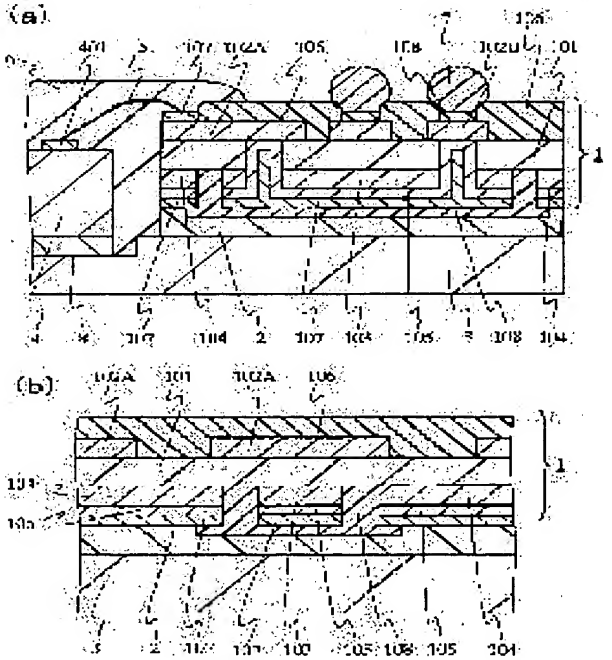
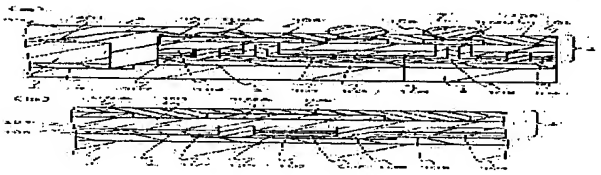
## (54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce a void generated on the bonding surface between a wiring tape and a heat sink in a TAB tape BGA type semiconductor device with double-sided wiring.
SOLUTION: An insulating binding material 2 and the heat sink 3 are provided on the back of a wiring tape 1 where first wiring 102A and an external connection terminal 102B are formed on the surface of an insulating base





101 having an open center section. A semiconductor chip 4 is provided in the opening of the base 101, and an external electrode 401 of the chip is connected to the first wiring 102A by a wire 5 for molding by resin 6. In a region other than second wiring 103 and its periphery on the back of the wiring tape 1, a ground layer 104 covered with a copper-plated layer 105 is provided, and the first wiring 102A on the surface of the base 101 is connected to the external connection terminal 102B via a via hole. Between the second wiring 103 and ground layer 104, an insulator 108 is provided while the insulator 108 sandwiches double plated layers 105 and 107.

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* NOTICES *



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CLAIMS

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[Claim(s)]
[Claim 1] The wiring tape on which the 1st wiring and its external connection terminal were formed in the 1st principal plane (side front side) of the insulating tape-like base material with which opening of the core was carried out is prepared. Make an insulator placed between the 1st principal plane (side front side) of said wiring tape, and the 2nd principal plane (background side) which counters, and a heat sink is prepared. Prepare a semiconductor chip in opening of said wiring substrate, and the external electrode of said semiconductor chip and said 1st wiring are connected by the bonding wire. In said semiconductor chip, a bonding wire, and the semiconductor device that comes to close those connections with resin Prepare the 2nd wiring in said 2nd principal plane of said wiring tape, and a touch-down potential layer (grand side) is prepared in the field except the perimeter of said 2nd wiring and said 2nd wiring. The semiconductor device characterized by preparing the flow beer which connects said 2nd wiring, a touch-down potential layer and said 1st wiring, and its external connection terminal in the predetermined location of said tape base material, and forming the insulator which insulates between said touch-down potential layers with said 2nd wiring in the perimeter of said 2nd wiring.
[Claim 2] The semiconductor device characterized by preparing the golden (Au) plating layer in the front face of said 2nd wiring and a touch-down potential layer in said semiconductor device according to claim 1.
[Claim 3] The wiring tape formation process which forms the wiring tape on which the 1st wiring and its external connection terminal were formed on the 1st principal plane (side front side) of the insulating tape-like base material with which opening of the core was carried out, The insulator arrangement process which arranges the insulator of the shape of a film which has opening in the

location which laps with opening and the flat-surface target of said tape base material at the 1st principal plane (side front side) of said wiring tape, and the 2nd principal plane (background side) which counters, A heat sink is arranged to the field where said wiring tape of said insulator has been arranged, and the field which counters. The heat sink adhesion process of pasting up said wiring tape and heat sink, and the semiconductor chip loading process of carrying a semiconductor chip in opening of said wiring tape of said heat sink, The wiring connection process of connecting wiring of said wiring tape with the external electrode of said semiconductor chip by the bonding wire, In the manufacture approach of a semiconductor device equipped with the semiconductor chip of opening of said wiring substrate, a bonding wire, and the closure process that closes those connections said wiring tape formation process A conductive thin film is formed in each of the 1st principal plane of said tape base material, and the 2nd principal plane. Form a beer hole in the predetermined location of said tape base material from said 2nd principal plane side, form the 1st plating layer on said conductive thin film and in the interior of a beer hole, and the conductive thin film on said 2nd principal plane is etched. Form the 2nd wiring and a touch-down potential layer (grand side), form opening in the core of said wiring tape, and the conductive thin film on said 1st principal plane is etched. Form the 1st wiring and its external connection terminal, and a wiring protective coat is formed so that said 1st wiring and its external connection terminal may be partially exposed on said 1st principal plane. The manufacture approach of the semiconductor device characterized by forming the 2nd plating layer in the exposure of said 1st wiring and its external connection terminal, said 2nd wiring, and a touch-down potential layer front face, applying and stiffening a liquefied insulator around said 2nd wiring, and insulating between touch-down potential layers with said 2nd wiring.

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[Translation done.]

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention is applied to the semiconductor device of the tape BGA (Ball Grid Array) mold which pasted up the heat sink on the wiring tape about a semiconductor device and its manufacture approach, and relates to an effective technique.
[0002]
[Description of the Prior Art] Conventionally, there is a semiconductor device of the tape BGA (T-BGA is called hereafter) mold which used a thin wiring tape like a TAB (Tape Automated Bonding) tape for one of the semiconductor devices of a BGA mold.
[0003] As said T-BGA type of semiconductor device is shown in drawing 12 (a) and drawing 12 (b) The wiring tape (TAB tape) 1 on which 1st wiring 102A and its external connection terminal 102B were formed in the 1st principal plane (side front side) of the insulating tape-like base material 101 with which opening of the core was carried out is formed. To the 1st principal plane (side front side) of said wiring tape 1, and the 2nd principal plane (background side) which counters For example, make the insulator (binder) 2 which consists of thermosetting resin like epoxy system resin intervene, and a heat sink 3 is pasted up. A semiconductor chip 4 is pasted up in opening 1A of said wiring tape 1 of said heat sink 3. The external electrode 401 of said semiconductor chip 4 and said 1st wiring 102A are connected by the bonding wire 5, and it has composition which closed said semiconductor chip 4, bonding wires 5, and those connections with mold resin 6. Moreover, on external connection terminal 102B of said 1st wiring, the ball terminal 7 which consists of Pb-Sn system solder etc. is connected.
[0004] In said T-BGA type of semiconductor device, moreover, on said wiring

tape (TAB tape) 1 For example, using the wiring tape of 2 metal structures which formed wiring in both the 1st principal plane of said tape base material 101, and the 2nd principal plane, as shown in drawing 13 (a) and drawing 13 (b) 1st wiring 102A of signal wiring etc. and its external connection terminal 102B were prepared in the 1st principal plane (side front side) of said tape base material 101, and the 2nd wiring 103 of power-source wiring etc. is formed in the 2nd principal plane (background side) of said tape base material 101. Moreover, as shown in drawing 13 (a), the touch-down potential layer (grand side) 104 is formed in the field except the field around [ which was established in the 2nd principal plane of said tape base material 101 ] said 2nd wiring 103. On said 2nd wiring 103 and the touch-down potential layer 104, the copper-plating layer (the 1st plating layer) 105 is formed, and said copper-plating layer 105 is connected with said 1st wiring 102A and its external connection terminal 102B by the beer hole prepared in the predetermined location of said tape base material 101.

[0005] Moreover, in order that fields other than the connection parts of said 1st wiring 102A and external connection terminal 102B may protect wiring from a contaminant, a blemish, etc. from the outside, the wiring protective coats 106, such as solder resist (SR) and photograph solder resist (PSR), are formed. The plating layer (the 2nd plating layer) 107 to which the laminating of (Nickel nickel) plating layer and the golden (Au) plating layer was carried out in order to improve the wirebonding nature of said 1st wiring 102A and the soldered-joint nature of said external connection terminal 102B is formed in the connection of said 1st wiring 102A and its external connection terminal 102B.

[0006] Moreover, on the wiring tape (TAB tape) of said 2 metal structures, in case said adhesives are stuck, or in case said adhesives are stiffened, oxidizing the copper front face of the adhesion interface 103, i.e., the 2nd wiring, the touch-down potential layer 104, and the copper-plating layer 105 prepared in those front faces, and leading to generating of the scale by the oxygen which penetrated the oxygen or the ingredient which remained to each component, is predicted easily. The scale itself is a very brittle oxide, and since exfoliation within the scale occurs easily, the dependability of equipment falls. Therefore, in order to prevent oxidation of said 2nd wiring 103, the touch-down potential layer 104, and the copper-plating layer 105, it is necessary to form the plating layer 107 as shown in drawing 11 (b).

[0007] On the wiring tape (TAB tape) of said 2 metal structures In order to give nickel plating and gilding to the front face of 1st wiring 102A and external connection terminal 102B and to form the plating layer 107 in it for improvement in wirebonding nature and soldered-joint nature, By also giving nickel plating

and gilding to the front face of said 2nd wiring 103 and the touch-down potential layer 104, and forming the plating layer 107 in it, in case said plating layer 107 is formed Oxidation of said 2nd wiring 103, the touch-down potential layer 104, and the copper-plating layer 105 can be prevented cheaply, without increasing a production process.

[0008] Here, although adhesion with said adhesives 2 generally becomes low compared with the case of copper when the plating layer 107 is formed in the copper-plating layer 105 of the front face of said 2nd wiring 103 and the touch-down potential layer 104 and gilding processing of the front face is carried out, the 2 kgf/cm value of the Peel reinforcement used as the standard of dependability is securable enough by selecting suitably the ingredient used as said adhesives 2.

[0009] Spacing during wiring with which wiring formed in the wiring tape 1 which uses said T-BGA type of semiconductor device with the miniaturization of equipment adjoins each other while being made detailed is also becoming narrow, and generating of the noise by the mutual inductance during wiring if it electromagnetic-field-joins together and puts in another way during adjacent wiring becomes a problem. Having influence on the noise which is between said wiring and is produced at this time most is power-source wiring with which the potential difference with the electrical potential difference impressed to the signal wiring which occupies said the greater part of wiring supplies the large operating voltage of said semiconductor chip 4. Therefore, the noise by the mutual inductance between said signal wiring and power-source wiring is reduced by forming power-source wiring (the 2nd wiring 103) in the background of the 1st principal plane in which said signal wiring (1st wiring 102A) of said tape base material was formed, and keeping away said power-source wiring from signal wiring.

[0010] Moreover, there is a problem that resonance phenomena will occur and signal wave forms, such as a clock pulse, will be confused also between the signal wiring prepared on the 1st principal plane of said wiring tape (TAB tape) 1 if spacing of adjacent wiring becomes narrow. Therefore, as shown in drawing 13 (a), the touch-down potential layer (grand side) 104 is formed in the field except said 2nd wiring 103 and its perimeter of the 2nd principal plane of said wiring tape (TAB tape). Since an eddy current flows in the direction which negates the magnetic flux generated in said touch-down potential layer (grand side) 104 according to the current which flows to said 1st wiring 102A and the self-inductance of 1st wiring 102A, the mutual inductance during wiring, and a dielectric cross talk can be reduced seemingly, when a RF signal is impressed to said 1st wiring (signal wiring) 102, it is effective, and improvement in the speed

of the dependability of an electrical signal and the transmission speed of a signal can be attained, for example.

[0011]

[Problem(s) to be Solved by the Invention] However, in said Prior art, when pasting up a heat sink 3 through an insulator (binder) 2 using the wiring tape of 2 metal structures on the 2nd wiring 103 of said wiring tape 1, and the touch-down potential layer (grand side) 104, in order to use a sheet-like binder, as shown in drawing 13 (b), between said 2nd wiring 103 and the touch-down potential layer 104, a void 11 will be made and air will remain. Therefore, the air which remained in said void 11 expanded with the heat-treatment in a production process, and the heat produced from a semiconductor chip 4 while in use as a product, and there was a problem that the surrounding binder 2 of said 2nd wiring 103 exfoliated.

[0012] Moreover, since the adhesive property with said binder 2 was not necessarily good, the crack would advance and the wiring tape 1 and a binder 2 would finally exfoliate if a binder 2 exfoliates around said 2nd wiring 103 and a crack arises, the plating layer 107 of the front face of said 2nd wiring 103 and the touch-down potential layer 104 had the problem that the dependability of equipment fell.

[0013] The purpose of this invention is in the semiconductor device of the T-BGA mold which pasted up the heat sink on the wiring tape on which wiring was formed in both sides of a tape base material through the binder to offer the technique which can reduce the void produced in the adhesion side of said wiring tape and binder.

[0014] Other purposes of this invention are in the semiconductor device of the T-BGA mold which pasted up the heat sink on the wiring tape on which wiring was formed in both sides of a tape base material through the binder to offer the technique which can reduce the exfoliation in respect of adhesion of said wiring tape and binder.

[0015] As new along [ said ] this invention a description as the other purposes will become clear by description and the accompanying drawing of this specification.

[0016]

[Means for Solving the Problem] It will be as follows if the outline of invention indicated in this invention is explained.

[0017] (1) The 1st of the insulating tape-like base material with which opening of the core was carried out The wiring tape on which the 1st wiring and its external connection terminal were formed in the principal plane (side front side) is prepared. Make an insulator placed between the 1st principal plane (side front

side) of said wiring tape, and the 2nd principal plane (background side) which counters, and a heat sink is prepared. Prepare a semiconductor chip in opening of said wiring substrate, and the external electrode of said semiconductor chip and said 1st wiring are connected by the bonding wire. In said semiconductor chip, a bonding wire, and the semiconductor device that comes to close those connections with resin Prepare the 2nd wiring in said 2nd principal plane of said wiring tape, and a touch-down potential layer (grand side) is prepared in the field except the perimeter of said 2nd wiring and said 2nd wiring. It is the semiconductor device with which the flow beer which connects said 2nd wiring, a touch-down potential layer and said 1st wiring, and its external connection terminal is prepared in the predetermined location of said tape base material, and the insulator which insulates between said touch-down potential layers with said 2nd wiring is formed in the perimeter of said 2nd wiring.

[0018] In the semiconductor device of the T-BGA mold using the wiring tape (TAB tape) of 2 metal structures where wiring was formed in both sides of said 1st principal plane and the 2nd principal plane according to the means of the above (1) When a heat sink is pasted up on the 2nd principal plane of said wiring tape through an insulator (binder) by forming an insulator in the perimeter of the 2nd wiring of said wiring tape, and insulating between touch-down potential layers with said 2nd wiring, it can prevent making a void between said 2nd wiring and a touch-down potential layer. Therefore, it can prevent the heat-treatment in a production process, and a void's expanding with the heat generated from a semiconductor chip, and said 2nd wiring and 1st insulator exfoliating while in use. Moreover, since exfoliation of said 2nd wiring and insulator (binder) can be reduced, the exfoliation in respect of adhesion of a wiring tape and said 1st insulator can be reduced, and the dependability of equipment can be improved.

[0019] Moreover, on the wiring tape (TAB tape) of said 2 metal structures, in order to prevent oxidation on the front face of copper of the 2nd wiring 103 and the touch-down potential layer 104, it is necessary to perform plating processing. Since the wiring tape of said 2 metal structures gives nickel plating and gilding to the front face of the 1st wiring and an external connection terminal and forms a plating layer in it, in case said plating layer is formed, oxidation of said 2nd wiring and a touch-down potential layer can be protected cheaply, without increasing a production process by also giving nickel plating and gilding to the front face of said 2nd wiring and a touch-down potential layer, and forming a plating layer in it.

[0020] Here, although adhesion with said adhesives generally becomes low compared with the case of copper when a plating layer is formed in said 2nd

wiring and a touch-down potential layer and gilding processing of the front face is carried out, dependability is securable enough by selecting suitably the ingredient used as said adhesives.

[0021] (2) The wiring tape formation process which forms the wiring tape on which the 1st wiring and its external connection terminal were formed on the 1st principal plane (side front side) of the insulating tape-like base material with which opening of the core was carried out, The insulator arrangement process which arranges the insulator of the shape of a film which has opening in the location which laps with opening and the flat-surface target of said tape base material at the 1st principal plane (side front side) of said wiring tape, and the 2nd principal plane (background side) which counters, A heat sink is arranged to the field where said wiring tape of said insulator has been arranged, and the field which counters. The heat sink adhesion process of pasting up said wiring tape and heat sink, and the semiconductor chip loading process of carrying a semiconductor chip in opening of said wiring tape of said heat sink, The wiring connection process of connecting wiring of said wiring tape with the external electrode of said semiconductor chip by the bonding wire, In the manufacture approach of a semiconductor device equipped with the semiconductor chip of opening of said wiring substrate, a bonding wire, and the closure process that closes those connections said wiring tape formation process A conductive thin film is formed in each of the 1st principal plane of said tape base material, and the 2nd principal plane. Form a beer hole in the predetermined location of said tape base material from said 2nd principal plane side, form the 1st plating layer on said conductive thin film and in the interior of a beer hole, and the conductive thin film on said 2nd principal plane is etched. Form the 2nd wiring and a touch-down potential layer (grand side), form opening in the core of said wiring tape, and the conductive thin film on said 1st principal plane is etched. Form the 1st wiring and its external connection terminal, and a wiring protective coat is formed so that said 1st wiring and its external connection terminal may be partially exposed on said 1st principal plane. The 2nd plating layer is formed in the exposure of said 1st wiring and its external connection terminal, said 2nd wiring, and a touch-down potential layer front face, a liquefied insulator is applied and stiffened around said 2nd wiring, and between touch-down potential layers is insulated with said 2nd wiring.

[0022] According to the means of the above (2), the wiring tape (TAB tape) of 2 metal structures where wiring was formed in both sides of said 1st principal plane and the 2nd principal plane is formed. In case the semiconductor device of a T-BGA mold is manufactured using the wiring tape of said 2 metal structures After forming the 1st wiring and an external connection terminal in the 1st

principal plane of said wiring tape and forming the 2nd wiring and a touch-down potential layer (grand side) in the 2nd principal plane of said tape base material, By making the perimeter of the 2nd wiring of said wiring tape apply and harden a liquefied insulator, between said 2nd wiring and touch-down potential layers can be fill uped with said insulator. Therefore, since a void is not made between said 2nd wiring and a touch-down potential layer when a heat sink is pasted up through an insulator (binder) on said 2nd wiring and a touch-down potential layer at a subsequent process, exfoliation of said 2nd wiring by expansion of the void at the time of the heat-treatment in a production process and an insulator (binder) can be prevented.

[0023] Moreover, in case plating processing is partially performed for said 1st wiring and an external connection terminal, by performing plating processing to coincidence also at said 2nd wiring and a touch-down potential layer (grand side), oxidation of said 2nd wiring and a touch-down potential layer can be prevented for them, and exfoliation of said binder can be prevented for them. Moreover, since plating processing is carried out to coincidence, a production process cannot increase, but it can suppress that a manufacturing cost increases.

[0024] Hereafter, this invention is explained to a detail with the gestalt (example) of operation with reference to a drawing.

[0025] In addition, in the complete diagram for explaining an example, what has the same function attaches the same sign, and explanation of the repeat is omitted.

[0026]

[Embodiment of the Invention] Drawing 1 thru/or drawing 4 are the mimetic diagrams showing the outline configuration of the semiconductor device of one example by this invention. (Example) The top view of a semiconductor device and drawing 1 (b) drawing 1 (a) The sectional view in the A-A' line of drawing 1 (a), For the ** type top view and drawing 2 (b) which looked at drawing 2 (a) from the 1st principal plane side of a wiring tape, the rear-face Fig. of drawing 2 (a) and drawing 3 are [ the sectional view in the B-B' line of drawing 3 and drawing 4 (b) of the partial enlarged drawing of drawing 2 (b) and drawing 4 (a) ] the sectional views in the C-C' line of drawing 3 . In addition, the sectional view of drawing 1 (b) omits and shows the parallel slash (hatching), in order to make the configuration of the semiconductor device of this example easy to grasp.

[0027] In drawing 1 thru/or drawing 4 1 opening and 101 for a wiring tape and 1A A tape-like base material, 102A the external connection terminal of the 1st wiring, and 103 for the 1st wiring and 102B The 2nd wiring, A touch-down potential layer (grand side) and 105 104 A copper-plating layer (the 1st plating

layer), 106 -- a wiring protective coat and 107 -- a plating layer (the 2nd plating layer) and 108 -- an insulator and 2 -- an insulator (binder) and 3 -- for an external electrode and 5, as for mold resin and 7, a bonding wire and 6 are [ a heat sink and 4 / a semiconductor chip and 401 / a ball terminal and 8 ] adhesives.

[0028] The semiconductor device of this example is the 1st of the insulating tape-like base material 101 with which opening of the core was carried out as shown in drawing 1 and drawing 2 . The wiring tape 1 on which 1st wiring 102A and its external connection terminal 102B were formed in the principal plane (side front side), The heat sink 3 which an insulator 2 is made placed between the 1st principal plane (side front side) of said wiring tape 1, and the 2nd principal plane (background side) which counters, and is prepared in it, The bonding wire 5 which connects the semiconductor chip 4 prepared in opening 1A of said wiring tape 1, the external electrode 401 of said semiconductor chip 4, and said 1st wiring 102A, The closure of said semiconductor chip 4, bonding wires 5, and those connections is carried out with mold resin 6, and it is the semiconductor device of the tape BGA (T-BGA) mold with which the ball terminal 7 was formed on said external connection terminal 102B.

[0029] Moreover, said wiring tape (TAB tape) 1 used with the semiconductor device of this example As it is the TAB tape of 2 metal structures where wiring was formed in the 1st principal plane of said wiring tape, and both sides of the 2nd principal plane and is shown in drawing 3 and drawing 4 It is a touch-down potential layer to the field the 2nd wiring 103 is formed in said 2nd principal plane of said wiring tape 1, and excluding the perimeter of said 2nd wiring 103 and said 2nd wiring 103. (grand side) 104 is prepared. Moreover, as said 2nd wiring 103 and the touch-down potential layer 104 are shown in drawing 4 , the copper-plating layer (the 1st plating layer) 105 is formed in the front face. Said copper-plating layer 105 is connected with said 1st wiring 102A and its external connection terminal 102B through the beer hole prepared in the predetermined location of said tape base material 101.

[0030] Moreover, parts other than the connection of 1st wiring 102A formed on the 1st principal plane of said wiring tape 1 and external connection terminal 102B are protected by wiring protective coat 106 like solder resist (SR) and photograph solder resist (PSR).

[0031] Moreover, the plating layer (the 2nd plating layer) 107 which carried out the laminating of a nickel-plating layer and the gilding layer is formed in the connection of said 1st wiring 102A and its external connection terminal 102B. Moreover, said plating layer 107 is formed also in the front face of the copper-plating layer 105 on said 2nd wiring 103 and the touch-down potential

layer (grand side) 104. Moreover, the insulator 108 which insulates between said touch-down potential layers 104 with said 2nd wiring 103 is formed in the perimeter of said 2nd wiring 103.

[0032] Moreover, as for the insulator (binder) 2 on which said wiring tape 1 and heat sink 3 are pasted up, thermosetting epoxy system resin etc. is used.

[0033] Moreover, in order that said heat sink 3 may operate the heat generated with said semiconductor chip 4 also as reinforcing materials of said wiring tape 1 while radiating heat efficiently, ingredients, such as copper (Cu), are used.

[0034] In the semiconductor device of the T-BGA mold of this example, the insulator 108 with which the circumference of the 2nd wiring 103 of said wiring tape 1 insulates between said touch-down potential layers 104 with said 2nd wiring 103 as shown in drawing 3 and drawing 4 is formed. Therefore, since a void does not arise between said 2nd wiring 103 and the touch-down potential layer 104 when pasting up said heat sink 3 through said insulator (binder) 2 on the 2nd wiring 103 of said wiring tape 1, and the touch-down potential layer 104, it can prevent a void's expanding with the heat generated from a semiconductor chip 4, and exfoliation of the adhesion side of said 2nd wiring 103 and insulator (binder) 2 arising while in use, for example. Moreover, even when the plating layer 107 on said 2nd wiring 103 and the touch-down potential layer (grand side) 104 and the adhesive strength of the adhesion side of an insulator (binder) 2 are weak, exfoliation in said 2nd wiring 103 part can be prevented, and it can prevent the wiring tape 1 and insulator 2 by advance of a crack from the exfoliation part exfoliating.

[0035] Drawing 5 thru/or drawing 10 are the mimetic diagrams in each production process for explaining the manufacture approach of the semiconductor device of this example. In addition, drawing 5 (b), drawing 6 , drawing 8 (b), and drawing 9 (b) show the sectional view equivalent to the cross section in the B-B' line of drawing 3 .

[0036] Hereafter, along with drawing 5 thru/or drawing 10 , the manufacture approach of the semiconductor device of this example is explained. In addition, the manufacture approach of the wiring tape (TAB tape) 1 used by this example For example "Reference Norio Okabe and Yasuhiro Kameyama and Hiroki Tanaka, Katsutoshi Taga and "2 Metal Layer TBGA Tape for High Speed, High Pin Count LSI Packaging", HITACHI CABLE REVIEW, and No.16 (August 1997), Since it is almost the same as that of the manufacture approach of the wiring tape of 2 conventional metal structures which were indicated by 49-54" etc., detailed explanation of each process is omitted.

[0037] First, in order to manufacture the wiring tape (TAB tape) of 2 metal

structures used with the semiconductor device of this example, as shown in drawing 5 (a) and drawing 5 (b), the tape 9 with copper foil on which the conductive thin films 109A and 109B, such as copper foil, were formed in both sides of an insulating tape base material like polyimide is prepared. Said tape with copper foil is obtained the thing which made for example, rolling copper foil rival with adhesives to both sides of the tape base material 101, and by vapor-depositing copper on said tape base material 101 by sputtering etc., and forming a thin film. Said tape 9 with copper foil is the thing of the shape of a long and slender tape, and wiring tape formation field 1' as shown in drawing 5 (a) is prepared in succession two or more.

[0038] As shown in drawing 6 (a), in the predetermined location of said tape 9 with copper foil next, by for example, carbon dioxide gas laser After forming the beer hole 10 which is one side and which while will be involved a principal plane (the 2nd principal plane), and reaches the conductive thin film of a principal plane (the 1st principal plane), as shown in drawing 6 (b), the copper (Cu) plating layer 105 is formed in the whole 2nd principal plane surface and the side face of said beer hole 10 as the 1st plating layer. Said copper plating is formed by the approach which combined for example, the electrolysis galvanizing method or the nonelectrolytic plating method, and the electrolysis galvanizing method.

[0039] Next, the 2nd principal plane side of said tape 9 with copper foil, the field which carried out opening of said beer hole 10 is etched, and in other words, as shown in drawing 6 (c), the touch-down potential layer (grand side) 104 except the field around the 2nd wiring 103 and said 2nd wiring 103 is formed. In addition, said 2nd wiring 103 and the touch-down potential layer 104 are formed by the pattern as shown in drawing 2 (b).

[0040] Next, as are shown in drawing 7 (a), and opening 1A is formed, and said conductive thin film 109A is etched after that and it is shown in drawing 7 (a) and drawing 7 (b) by carbon dioxide gas laser etc., 1st wiring 102A and its external connection terminal 102B are formed in the center section of said wiring substrate formation field 1'. In addition, although the part is omitted in drawing 7 (a), each external connection terminal 102B is taken about around said opening 1A through 1st wiring 102A, direct, or the 2nd wiring.

[0041] Next, as shown in drawing 8 (a), in order to protect said 1st wiring 102A and its external connection terminal 102B from the contaminant and blemish from the outside, a wiring protective coat 106 like solder resist or photograph solder resist is formed.

[0042] Next, using the electrolysis galvanizing method, a nonelectrolytic plating

method, or electroplating, as shown in drawing 8 (b), the plating layer (the 2nd plating layer) 107 for improving the wirebonding nature of said 1st wiring 102A and the soldered-joint nature of external connection terminal 102B is formed. At this time, in order to prevent oxidation, the plating layer 107 is formed also in the front face of the 2nd wiring 103 of said 2nd principal plane, and the copper-plating layer 105 on the touch-down potential layer 104 at coincidence. Said plating layer 107 carries out the laminating of for example, (Nickel nickel) plating layer and the golden (Au) plating layer, and forms them.

[0043] Next, as shown in drawing 9 (a) and drawing 9 (b), if a liquefied insulator 108 like solder resist (SR) is applied and stiffened, the wiring tape (TAB tape) 1 of 2 metal structures used with the semiconductor device of the T-BGA mold of this example will be formed around said 2nd wiring 103.

[0044] As shown in drawing 10 (a) and drawing 10 (b), next, on said 2nd wiring 103 of said wiring tape 1, and the touch-down potential layer 104 A heat sink 3 is arranged to the field where the insulator (binder) 2 of the shape of a film which has opening in the location which laps with opening 1A of said wiring tape 1 superficially has been arranged, and said wiring tape 1 of said insulator 2 has been arranged, and the field which counters, and said wiring tape 1 and heat sink 3 are pasted up. Although it heat-treats in order to paste up said wiring tape 1 and heat sink 3 since thermosetting epoxy system resin etc. is used as said insulator (binder) 2 at this time Since it is buried by the insulator 108 between the 2nd wiring 103 of said wiring tape 1, and the touch-down potential layer (grand side) 104, it does not have a void, and it can prevent exfoliation of said 2nd wiring 103 by expansion of the void at the time of heating and an insulator (binder) 2. Moreover, in order that said insulator (binder) 2 may improve adhesion with gilding of said 2nd wiring 103 and touch-down potential layer 104 front face at this time, the amount of the charge of a principal member and an additive is adjusted suitably, and it enables it to acquire predetermined adhesion dependability.

[0045] Next, as shown in drawing 11 (a) and drawing 11 (b), a semiconductor chip 4 is carried in opening 1A of said wiring tape of said heat sink 3, and 1st wiring 102A of said wiring tape 1 is connected with the external electrode 401 of said semiconductor chip 4 by the bonding wire 5.

[0046] Then, if the ball terminal 7 is connected on said external connection terminal 102B after closing the semiconductor chip 4, the bonding wires 5, and those connections in opening 1A of said wiring tape 1 by mold resin 6, the semiconductor device of the T-BGA mold of this example as shown in drawing 1 thru/or drawing 4 can be obtained. Moreover, also at this time, in case said ball

terminal 7 is connected, although it heats and said ball terminal 7 is dissolved partially, since there is no void between said 2nd wiring 103 and the touch-down potential layer 104, exfoliation of said 2nd wiring 103 and insulator (binder) 2 can be prevented.

[0047] As explained above, in the semiconductor device of this example Around the 2nd wiring 103 formed in the field which the heat sink 3 of said wiring tape (TAB tape) 1 pastes up By applying and stiffening the liquefied insulator 105 and fill uping with said insulator 105 between the touch-down potential layers (grand side) 104 prepared in the perimeter of said 2nd wiring 103 and said 2nd wiring 103 When the sheet-like insulator (binder) 2 is pasted up on said 2nd wiring 103 and the touch-down potential layer 104, a void can be prevented from being made to the perimeter of said 2nd wiring 103. Therefore, it can prevent the air which remained in said void expanding and the adhesion side of said 2nd wiring 103 and insulator (binder) 2 exfoliating by heat-treatment in a production process. Moreover, since the exfoliation in respect of adhesion of said 2nd wiring 103 and insulator (binder) 2 can be prevented and generating of the crack in the adhesion side of said wiring tape 1 and insulator 2 can be lessened, the defect of the semiconductor device by exfoliation of said wiring tape 1 and insulator 2 can be reduced.

[0048] By moreover, the thing for which the same plating layer 107 also as the front face of said 2nd wiring 103 and the touch-down potential layer 104 is formed in case a plating layer is formed on said 1st wiring 102A and its external connection terminal 102B Since oxidation of said 2nd wiring 103 and the touch-down potential layer 104 can be prevented, peeling in respect of adhesion with said binder 2 by oxidation of said 2nd wiring 103 and the touch-down potential layer 104 can be prevented, and the defect of a semiconductor device can be prevented.

[0049] As mentioned above, although this invention was concretely explained based on said example, as for this invention, it is needless to say for it to be able to change variously in the range which is not limited to said example and does not deviate from the summary.

[0050]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this invention is explained briefly.

[0051] (1) In the semiconductor device of the T-BGA mold which pasted up the heat sink on the wiring tape on which wiring was formed in both sides of a tape base material through the binder, it can prevent a void arising in the adhesion side of said wiring tape and binder.

[0052] (2) In the semiconductor device of the T-BGA mold which pasted up the

heat sink on the wiring tape on which wiring was formed in both sides of a tape base material through the binder, the exfoliation in respect of adhesion of said wiring tape and binder can be reduced.

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[Translation done.]